

Claim 6
6 where n and m are integers.

1 2. (Once Amended) The crossbar device of claim 1, wherein at least one of the
2 plurality of chains of pass transistors consists of a first and a second pass transistor.

1 3. (Once Amended) The crossbar device of claim 1, wherein each of the plurality of
2 chains of pass transistors consists of a first and a second pass transistor.

Claim 5
1 5. (Once Amended) The crossbar device of claim 1, wherein the device further
2 comprises a plurality of p to q decoder logics coupled to the input lines, where p and
3 q are integers, with p being less than q.

Claim 7
1 7. (Once Amended) A reconfigurable circuit comprising:
2 a plurality of crossbar devices coupled to one another, each crossbar device
3 having at least a memory element, and an output buffer electrically associated with
4 the memory element; and
5 a voltage supply structure coupled to the crossbar device designed to supply
6 Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the
7 memory elements to maintain the input voltage of the output buffers at Vdd.

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1 8. (Once Amended) The reconfigurable circuit of claim 7, wherein at least one of the
2 plurality of crossbar devices comprises:
3 n input line;
4 m output lines; and
5 a plurality of chains of pass transistors coupling the n input lines to the m
6 output lines;
7 where n and m are integers.

1 9. (Once Amended) The reconfigurable circuit of claim 8, wherein at least one of the
2 plurality of chains of pass transistors consists of a first and a second pass transistor.

1 10. (Once Amended) The reconfigurable circuit of claim 8, wherein each of the
2 plurality of chains of pass transistors consists of a first and a second pass transistor.

1 11. (Once Amended) The reconfigurable circuit of claim 7, wherein each of the
2 plurality of crossbar devices comprises:
3 n input line;
4 m output lines; and
5 a plurality of chains of pass transistors coupling the n input lines to the m
6 output lines;
7 where n and m are integers.

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1 15. (Once Amended) A reconfigurable circuit comprising:
2 a plurality of crossbar devices coupled to one another, each crossbar device
3 having at least an output buffer; and
4 a power-on circuitry coupled to the crossbar devices to force the output
5 buffers to a known logic value at power-on.

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1 17. (Once Amended) The reconfigurable circuit of claim 15, wherein at least one of
2 the plurality of crossbar devices comprises:
3 n input lines;
4 m output lines; and
5 a plurality of chains of pass transistors coupling the n input lines to the m
6 output lines;
7 where n and m are integers.

1 18. (Once Amended) The reconfigurable circuit of claim 17, wherein at least one of
2 the plurality of chains of pass transistors consists of a first and a second pass
3 transistor.

1 19. (Once Amended) The reconfigurable circuit of claim 17, wherein each of the
2 plurality of chains of pass transistors consists of a first and a second pass transistor.

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1 20. (Once Amended) The reconfigurable circuit of claim 15, wherein each of the
2 plurality of crossbar devices comprises:
3 n input line;
4 m output lines; and
5 a plurality of chains of pass transistors coupling the n input lines to the m
6 output lines;
7 where n and m are integers.

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1 22. (Once Amended) The reconfigurable circuit of claim 15, wherein
2 each crossbar device further having at least a memory element electrically
3 associated to an output buffer; and
4 the reconfigurable circuit further comprises a voltage supply structure coupled
5 to the crossbar devices designed to supply Vdd to the output buffers, and a voltage
6 raised by a threshold over Vdd to the memory elements to maintain the voltage
7 supply of the output buffers at Vdd.

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REMARKS

Summary of the Office Action

In the present application, claims 1-24 stand rejected. In addition, the drawings, specification and claims where objected to due to informalities.